Signetics

# 27C256

## 256K CMOS UV Erasable PROM (32K × 8)

***Product Specification***

**Military Application Specific Products**

### DESCRIPTION

The Signetics 27C256 CMOS EPROMs are 256K-Bit 5V only memories organized as 32,768 words of 8 bits. They employ advanced CMOS circuitry for systems requiring low-power, high-performance speeds and immunity to noise. The 27C256 has a non-multiplexed addressing interface and is plug compatible with the industry standard 27256.

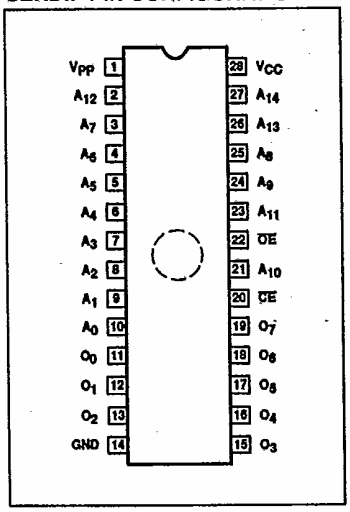
The 27C256 achieves both high-performance and low power consumption (10mA active current maximum, CMOS inputs), making them ideal for high-performance, portable equipment.

It is programmed with standard EPROM programmers and the intelligent programming algorithm may be utilized.

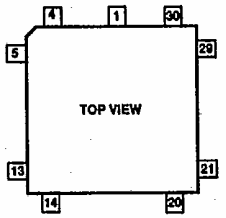
### FEATURES

- **CMOS/NMOS microcontroller and microprocessor compatible**
  - **Universal 28- or 32-Pin memory site, 2-line control**
- **Low power consumption**
- **Noise immunity features**
  - **±10% $V_{CC}$ tolerance**
  - **Maximum latch-up immunity through epitaxial processing**
- **Fast, reliable intelligent programming**
  - **12.5V $V_{PP}$, HCMOS 11-E compatible**

### CERDIP PIN CONFIGURATION




### LLCC PIN CONFIGURATION




PIN/FUNCTION

| | | | | | |
|---|---|---|---|---|---|
| 1 | NC | 12 | NC | 23 | $\overline{OE}$ |
| 2 | $V_{PP}$ | 13 | $O_0$ | 24 | $A_{10}$ |
| 3 | $A_{12}$ | 14 | $O_1$ | 25 | $\overline{CE}$ |
| 4 | $A_7$ | 15 | $O_2$ | 26 | NC |
| 5 | $A_6$ | 16 | $V_{SS}$ | 27 | $A_{11}$ |
| 6 | $A_5$ | 17 | NC | 28 | $A_9$ |
| 7 | $A_4$ | 18 | $O_3$ | 29 | $A_8$ |
| 8 | $A_3$ | 19 | $O_4$ | 30 | $A_{13}$ |
| 9 | $A_2$ | 20 | $O_5$ | 31 | $A_{14}$ |
| 10 | $A_1$ | 21 | $O_6$ | 32 | $V_{CC}$ |
| 11 | $A_0$ | 22 | $O_7$ | | |

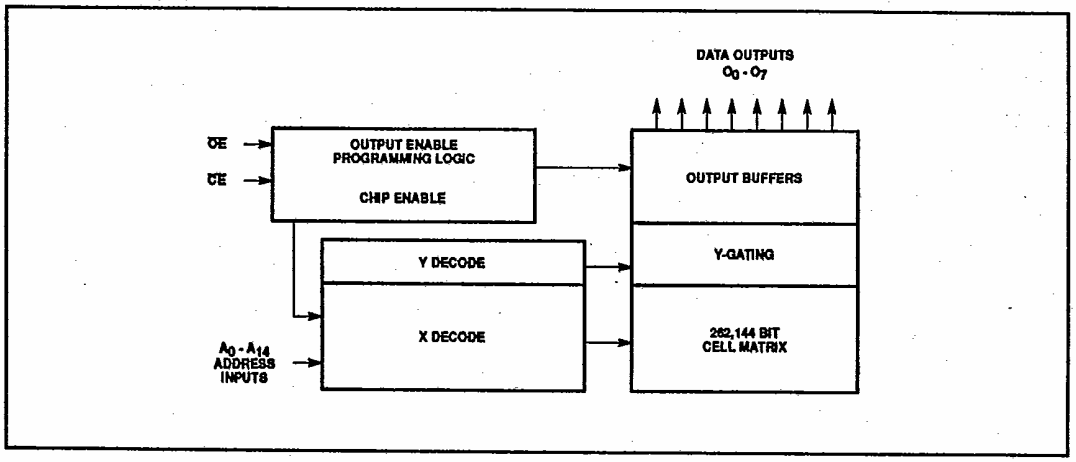
### PIN NAMES

| | |
|---|---|
| $A_0$ - $A_{14}$ | Addresses |
| $O_0$ - $O_7$ | Outputs |
| $\overline{OE}$ | Output Enable |
| $\overline{CE}$ | Chip Enable |
| GND | Ground |
| $V_{PP}$ | Program Voltage |
| $V_{CC}$ | Power Supply |

### ORDERING INFORMATION

| PACKAGES | ORDER CODE | | |
|---|---|---|---|
| | 150ns | 200ns | 250ns |
| 28-Pin Ceramic DIP w/Quartz Window | 27C256/BXA-15 | 27C256/BXA-20 | 27C256/BXA-25 |
| 28-Pin Ceramic DIP w/o Quartz Window[1] | 27C256/BXA-15 OT | 27C256/BXA-20 OT | 27C256/BXA-25 OT |
| 32-Pin Rectangular LLCC w/Quartz Window | 27C256/BUA-15 | 27C256/BUA-20 | 27C256/BUA-25 |

## BLOCK DIAGRAM




## ABSOLUTE MAXIMUM RATINGS[2]

| SYMBOL | PARAMETER | RATING | UNIT |
|---|---|---|---|
| $T_{STG}$ | Storage temperature range | -65 to +150 | °C |
| $V_I$, $V_O$ | Voltage on any pin with respect to ground | -2.0 to $V_{CC}$ +7V | V |
| $V_I$ | Voltage on $\overline{CE}$ Pin with respect to ground | -2.0 to +13.5 | V |
| $V_{PP}$ | Supply voltage with respect to ground during programming | -2.0 to 14.0 | V |

## RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Nom | Max | |
| $V_{CC}$ | Supply voltage | | 4.5 | 5.0 | 5.5 | V |
| $V_{IH}$[3] | High-level input voltage | | 2.0 | | $V_{CC}$ + 0.5[12] | V |
| $V_{IH}$[3] | High-level input voltage CMOS | $V_{PP} = V_{CC}$ | $V_{CC}$ - 0.2 | | $V_{CC}$ + 0.2[12] | V |
| $V_{IL}$[3] | Low-level input voltage | $V_{PP} = V_{CC}$ | -0.5[12] | | 0.8 | V |
| $V_{IL}$[3] | Low-level input voltage CMOS | $V_{PP} = V_{CC}$ | -0.2[12] | | 0.2 | V |
| $I_{OH}$ | High-level output current | | | | -400 | µA |
| $I_{OL}$ | Low-level output current | | | | 2.1 | mA |
| $V_{PP}$ | $V_{PP}$ read voltage [8] | | $V_{CC}$ - 0.7 | | $V_{CC}$ | V |
| $T_A$ | Operating temperature range | | -55 | | +125 | °C |

## READ OPERATION DC CHARACTERISTICS $-55\,°C \le T_A \le +125°C$, $V_{CC} = 5V \pm 10\%$

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|---|---|---|---|---|---|---|
| | | | Min | Typ[4] | Max | |
| $I_{LIH}$ | Input leakage current | $V_I = V_{CC}$ = Max | | 0.01 | +1.0 | µA |
| $I_{LIL}$ | | $V_I$ = 0.0V | | | -1.0 | µA |
| $I_{OIH}$ | Output leakage current | $V_I = V_{CC}$ = Max | | 0.01 | +1.0 | µA |
| $I_{OIL}$ | | $V_I$ = 0.0V | | | -1.0 | µA |
| $I_{CC}TTL^{6,8}$ | Operating current TTL inputs | $\overline{CE} = \overline{OE}$ - $V_{IL}$, $V_{PP} = V_{CC}$ - Max $O_0$ - $O_7$ = 0mA | | | 30 | mA |
| $I_{CC}CMOS^{6,8}$ | Operating current CMOS inputs | $\overline{CE} = \overline{OE}$ - $V_{IL}$, $V_{PP} = V_{CC}$ - Max $O_0$ - $O_7$ = 0mA | | | 10 | mA |
| $I_{SB}TTL^{8}$ | Standby current TTL inputs | $\overline{CE} = V_{IH}$ | | | 2 | mA |
| $I_{SB}CMOS^{5}$ | Standby current CMOS inputs | $\overline{CE} = V_{IH}$ | | | 100 | µA |
| $I_{PP}{}^{8}$ | $V_{PP}$ read current | $V_{PP} = V_{CC}$ = Max | | | 200 | µA |
| $V_{IL}{}^{9}$ | Input Low voltage (TTL)<br>Input Low voltage (CMOS) | $V_{PP} = V_{CC}$ | -0.5[10]<br>-0.2[10] | | 0.8<br>0.2 | V<br>V |
| $V_{IH}{}^{9}$ | Input High voltage (TTL)<br>Input High voltage (CMOS) | $V_{PP} = V_{CC}$ | 2.0<br>$V_{CC}$ -0.2 | | $V_{CC}$ + 0.5[10]<br>$V_{CC}$ + 0.2[10] | V<br>V |
| $V_{OL}$ | Output Low voltage | $I_{OL}$ = Max | | | 0.45 | V |
| $V_{OH}$ | Output High voltage | $I_{OH}$ = Max | 2.4 | | | V |
| $I_{OS}{}^{7}$ | Output short-circuit current | | | | -100 | mA |

## CAPACITANCE $T_A = 25°C$, f = 1.0MHz

| SYMBOL | PARAMETER | TEST CONDITIONS | MAX | UNIT |
|---|---|---|---|---|
| $C_I{}^{10}$ | Address/control capacitance | $V_I$ = 0V | 6 | pF |
| $C_O{}^{10}$ | Output capacitance | $V_O$ = 0V | 12 | pF |

## READ MODES

| MODE | PINS | | | |
|---|---|---|---|---|
| | $\overline{CE}$ (20) | $\overline{OE}$ (22) | $V_{PP}$ (1) | OUTPUTS (11-13, 15-19) |
| Read | $V_{IL}$ | $V_{IL}$ | $V_{CC}$ | $D_O$ |
| Output disable | $V_{IL}$ | $V_{IH}$ | $V_{CC}$ | Hi-Z |
| Standby | $V_{IH}$ | X | $V_{CC}$ | Hi-Z |

## READ MODE

The 27C256 has two control functions, both of which must be logically active in order to obtain data at the outputs. Chip Enable ($\overline{CE}$) is the power control and should be used for device selection. Output Enable ($\overline{OE}$) is the output control and should be used to gate data from the output pins, independent of device selection. Assuming that addresses are stable, the address access time ($t_{ACC}$) is equal to the delay from $\overline{CE}$ to output ($t_{CE}$). Data is available at the outputs after a delay of $t_{OE}$ from the falling edge of $\overline{OE}$, assuming that $\overline{CE}$ has been low and addresses have been stable for at least $t_{ACC}$-$t_{OE}$.

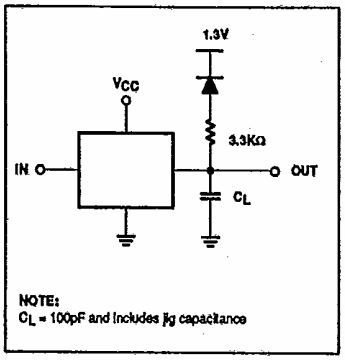
## STANDBY MODE

The 27C256 has a Standby mode which reduces the maximum CMOS V current to 100µA. The device is placed in the Standby mode when Pin 20 is in the High state. When in the Standby mode, the outputs are in a high-impedance state, independent of the $\overline{OE}$ input.

## READ OPERATION - AC CHARACTERISTICS $-55\,°C \le T_A \le +125°C$, $4.5V \le V_{CC} \le 5.5V$[12]

| SYMBOL | PARAMETER | 27C256-15 | | 27C256-20 | | 27C256-25 | | UNIT |
|---|---|---|---|---|---|---|---|---|
| | | Min | Max | Min | Max | Min | Max | |
| $t_{ACC}$ | Address to output delay | | 150 | | 200 | | 250 | ns |
| $t_{CE}$ | $\overline{CE}$ to output delay | | 150 | | 200 | | 250 | ns |
| $t_{OE}$ | $\overline{OE}$ to output delay | | 65 | | 75 | | 100 | ns |
| $t_{OP}$[10] | $\overline{OE}$ or $\overline{CE}$ High to output Hi-Z | | 45 | | 55 | | 60 | ns |
| $t_{OH}$[10] | Output hold from addresses, $\overline{CE}$ or $\overline{OE}$ change - whichever is first | 0 | | 0 | | 0 | | ns |

## AC TESTING LOAD CIRCUIT




NOTE:
$C_L$ = 100pF and includes jig capacitance

## SYSTEM CONSIDERATIONS

The power switching characteristics of CMOS EPROMs require careful decoupling of the devices. The supply current, $I_{CC}$, has three segments that are of interest to the system designer - the standby current level, the active current level, and the transient current peaks that are produced by the falling and rising edges of Chip Enable. The magnitude of these transient current peaks is dependent on the output capacitive and inductive loading of the devices. The associated transient voltage peaks can be suppressed by complying with Two-Line Control and by properly selected decoupling capacitors.

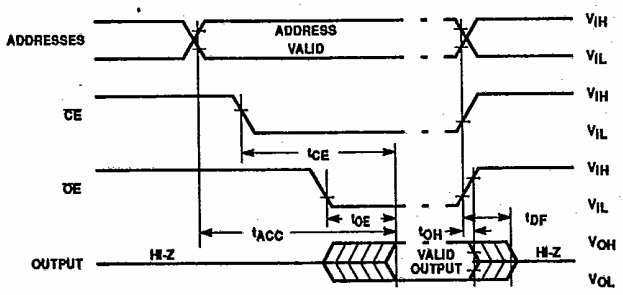
It is recommended that a 0.1µF ceramic capacitor be used on every device between $V_{CC}$ and GND. This should be a high frequency capacitor of low inherent inductance and should be placed as close to the device as possible. In addition, a 4.7µF bulk electrolytic capacitor should be used between $V_{CC}$ and GND for every eight devices. The bulk capacitor should be located near where the power supply is connected to the array. The purpose of the bulk capacitor is to overcome the voltage drop caused by the inductive effects of PC board traces.

## ERASURE CHARACTERISTICS

The erasure characteristics of the 27C256 are such that erasure begins to occur upon exposure to light with wavelengths shorter than approximately 4000 Angstroms (Å). It should be noted that sunlight and certain types of fluorescent lamps have wavelengths in the 3000-4000 Å Range. Data shows that constant exposure to room level fluorescent lighting could erase the typical 27C256 in approximately three years, while it would take approximately one week to cause erasure when exposed to direct sunlight. If the 27C256 is to be exposed to these types of lighting conditions for extended periods of time, opaque labels should be placed over the window to prevent unintentional erasure.

The recommended erasure procedure for the 27C256 is exposure to shortwave ultraviolet light which has a wavelength of 2537 Angstroms (Å). The integrated dose (i.e., UV intensity x exposure time) for erasure should be a minimum of 15Wsec/cm$^2$. The erasure time with this dosage is approximately 15 to 20 minutes using an ultraviolet lamp with a 12,000µW/cm$^2$ power rating. The 27C256 should be placed within one inch of the lamp tubes during erasure. The maximum integrated dose a 27C256 can be exposed to without damage is 7258W/cm$^2$ (1 week @ 1200µW/cm$^2$). Exposure of these CMOS EPROMs to high intensity UV light for longer periods may cause permanent damage.

## AC WAVEFORMS




Input Pulse Characteristics: $t_r$, $T_f \leq 5ns$, $P_{RR}$ = 1MHz

## PROGRAMMING MODES

| MODES | PINS | | | | | | |
|---|---|---|---|---|---|---|---|
| | $\overline{CE}$ (20) | $\overline{OE}$ (22) | $A_9$ (24) | $A_0$ (10) | $V_{PP}$ (1) | $V_{CC}$ (28) | OUTPUTS (11-13, 15-19) |
| Intelligent programming | $V_{IL}$ | $V_{IH}$ | X[13] | X[13] | $V_{PP}$ | 6.0V[16] | $D_1$ |
| Program verify | $V_{IH}$ | $V_{IL}$ | X[13] | X[13] | $V_{PP}$ | 6.0V[16] | $D_2$ |
| Program inhibit | $V_{IH}$ | $V_{IH}$ | X[13] | X[13] | $V_{PP}$ | 6.0V[16] | Hi-Z |
| Intelligent identifier-manufacturer[15] | $V_{IL}$ | $V_{IL}$ | $V_H$[14] | $V_{IL}$ | $V_{CC}$ | $V_{CC}$ | 15H |
| Intelligent identifier[15] | $V_{IL}$ | $V_{IL}$ | $V_H$[14] | $V_{IH}$ | $V_{CC}$ | $V_{CC}$ | 8CH |

## CMOS NOISE CHARACTERISTICS

Special epitaphial processing techniques have enabled Signetics to build CMOS with features adding to system reliability. These include Input/Output protection to latch-up. Each of the data and address pins will not latch-up with currents up to 100mA and voltages from -1V to $V_{CC}$ + 1V.

Additionally, the $V_{PP}$ (Programming) pin is designed to resist latch-up to the 14V maximum device limit.

## PROGRAMMING

***Caution:*** Exceeding 14.0V on $V_{PP}$ Pin may permanently damage the 27C256.

Initially, and after each erasure, all bits of the 27C256 are in the "1" state. Data is introduced by selectively programming "0" into the desired bit location. Although only "0" will be programmed, both "1" and "0" can be present in the data word. The only way to change an "0" to a "1" is by ultraviolet light erasure.

The 27C256 is in the programming mode when the $V_{PP}$ input is at 12.5V and $\overline{CE}$ is at TTL-Low. The data to be programmed is applied 8 bits in parallel to the data output pins. The levels required for the address and data inputs are TTL.

## INTELLIGENT PROGRAMMING™ ALGORITHM

The 27C256 intelligent programming algorithms rapidly program Signetics CMOS EPROMs using an efficient and reliable method particularly suited to the production programming environment. Typical programming times for individual devices are on the order of five minutes. Actual programming times may vary due to differences in programming equipment.

Programming reliability is also ensured as the incremental program margin of each byte is continually monitored to determine when it has been successfully programmed. A flow-chart of the 27C256 intelligent program algorithm is shown in Figure 1.

The intelligent programming algorithm utilizes two different pulse types: initial and overprogram. The duration of the initial $\overline{CE}$ pulse(s) is 1ms, which will then be followed by a longer overprogram pulse of length 3Xms. X is a duration counter and is equal to the number of the initial 2ms pulses applied to a particular 27C256 location, before a correct verify occurs. Up to 25 1ms pulses per byte are provided for before the overprogram is applied.

The entire sequence of program pulses and byte verifications is performed at $V_{CC}$ = 6.0V and $V_{PP}$ = 12.5V.

When the intelligent programming cycle has been completed, all bytes should be compared to the original data with $V_{CC}$ = 5.0V.

## PROGRAM INHIBIT

Programming of multiple 27C256 EPROMs in parallel with different data is easily accomplished by using the Program Inhibit mode. A high-level $\overline{CE}$ input inhibits other 27C256 EPROMs from being programmed.

Except for $\overline{OE}$ or $\overline{CE}$, all inputs of the parallel 27C256s may be common. A TTL low-level pulse applied to the $\overline{CE}$ or ALE/$\overline{CE}$ input with $V_{PP}$ at 12.5V will program the selected 27C256.

## VERIFY

A verify (read) should be performed on the programmed bits to determine that they have been correctly programmed. The verify is performed with $\overline{OE}$ at $V_{IL}$ and $\overline{CE}$ at $V_{IH}$ and $V_{PP}$ at 12.5V.

Data should be verified a minimum of $T_{OEV}$ after the falling edge of $\overline{OE}$.

16. $V_{CC}$ = 6.0V ± 0.25V.
17. AC Conditions of Test:
    Input Rise and Fall Times (100% to 90%): 20ns
    Input Pulse Levels: 0.45V to 2.4V
    Input Timing Reference Level: 0.8V to 2.0V
    Output Timing Reference Level: 0.8V to 2.0V
18. Initial Program Pulse width tolerance is 1msec ± 5%.
19. The length of the overprogram pulse may vary from 2.85msec to 78.75msec as a function of the iteration counter value X.
20. This parameter is only sampled and is not 100% tested. Output Float is defined as the point where data is no longer driven (see Timing Diagram).

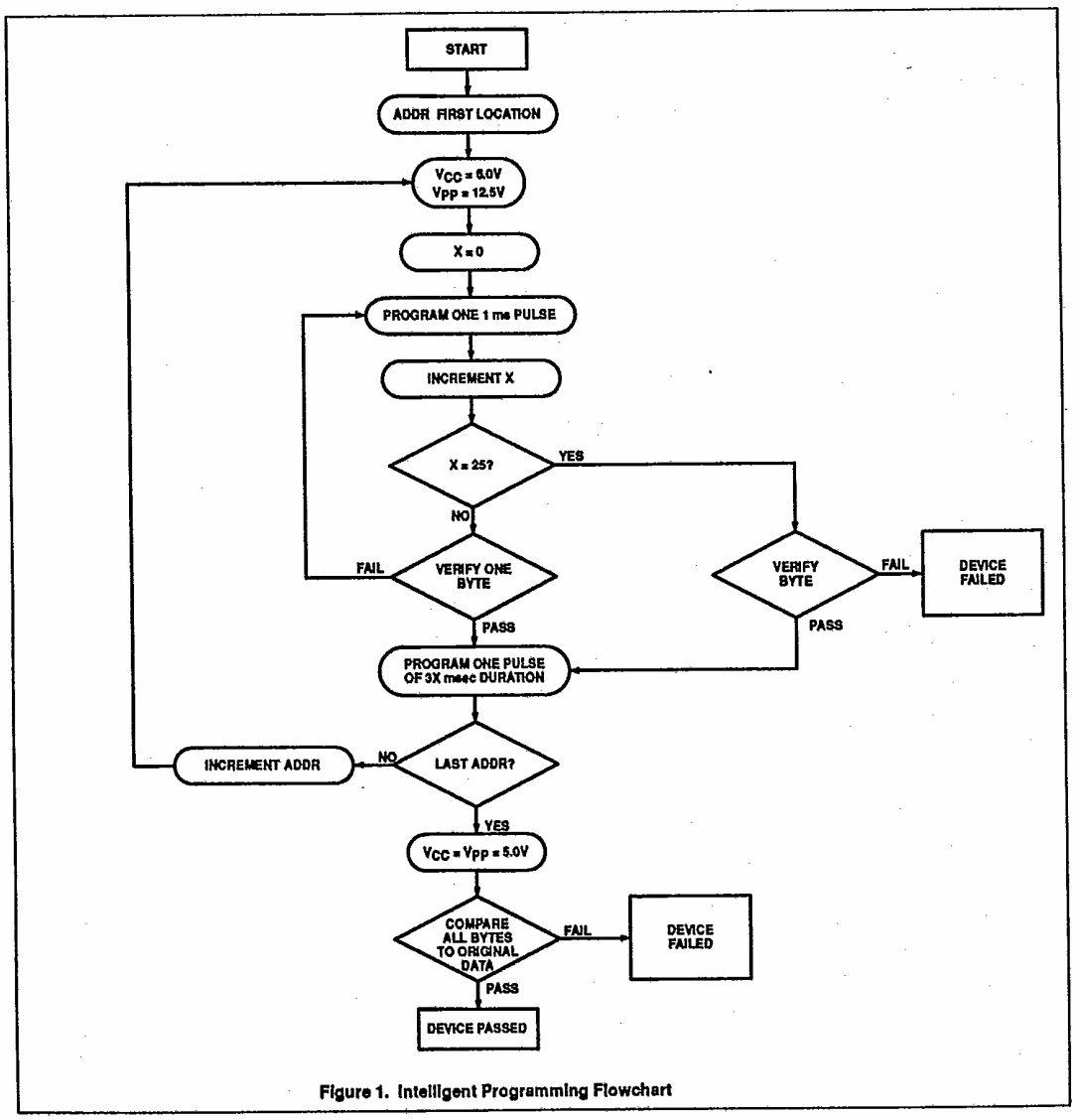
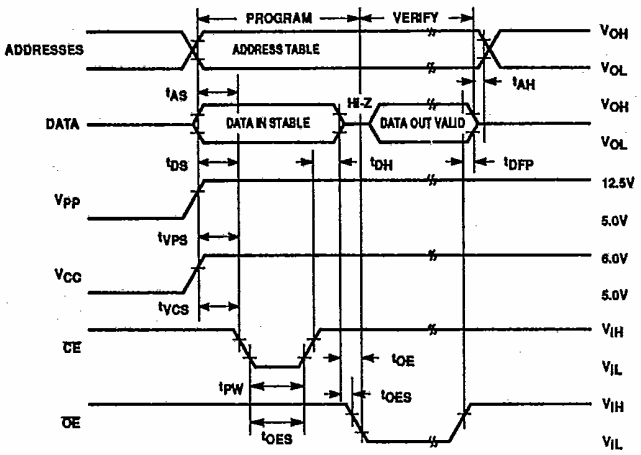



**Figure 1. Intelligent Programming Flowchart**




NOTES:
1. The Input Timing Reference Level is 0.8V for $V_{IL}$ and 2V for a $V_{IH}$, input pulse levels are 0.45V and 2.4V.
2. $t_{OE}$ and $t_{DFP}$ are characteristics of the device but must be accommodated by the programmer.
3. When programming 27C256, a 0.1uF capacitor is required across $V_{PP}$ and ground to suppress spurious voltage transients which can damage the device.

**Figure 2. Intelligent Programming Waveforms**